REMARKS/ARGUMENTS

The amendment is in response to the Final Office Action dated August 23, 2005 and the Advisory Action dated October 14, 2005. Claims 1 and 4-20 are pending in the present application. Claims 1, 4-6, and 8-15 have been changed, claims 2 and 3 have been cancelled, and claims 16-20 have been added by this amendment.

No new matter or new issues have been presented. The amendments to claims 1 and 9 are supported by Applicant's specification at, for example, Fig. 2 and on page 4, lines 13-21. The amendments to claims 4-6, 8, and 10-15, and new claims 16-20, are supported by Applicant's specification at, for example, pages 3-4 and Fig. 2.

The 102 Rejections

The Examiner rejected claims 1-15 under 35 U.S.C. §102(e) as being anticipated by Chang et al. (U.S. Patent No. 6,636,077) ("Chang"). Applicant has amended claims 1 and 9 for clarification, and the claims dependent thereon for clarification and consistency with the independent claims.

Applicant's claim 1 recites a multiplexer comprising a first input, a first differential amplifier of a first channel including a first differential pair of transistors coupled to the first input, a second input, a second differential amplifier of a second channel including a second differential pair of transistors coupled to the second input, an output, a first plurality of selection transistors coupled between first differential pair and output, and a second plurality of selection transistors coupled between second differential pair and output. The first channel is selected as active or inactive by the first plurality of selection transistors, and the second channel is selected as active or inactive by the second plurality of selection transistors.

Chang does not disclose or suggest a multiplexer in which such selection transistors are coupled between the differential amplifiers and the output. In Chang's circuit of Fig. 2, the differential amplifiers are transistor pairs 286-288, 290-292, 294-296, and 298-211, as disclosed in col. 3, lines 39-46. Chang also includes buffer transistor pairs 206-208, 210-212, 214-216, and 218-220 (col. 3, lines 44-54). Chang's transistors 286-288, etc. of the differential amplifiers are all coupled directly to the output OUT and OUTB, and there are no transistors coupled between these differential amplifiers and the output. Furthermore, Chang's selection transistors, which select the channels (Ch0, Ch1, etc.) as active or inactive, are the "control transistors" which "select the proper channel based upon inputs C and S" (col. 2, lines 47-48). For example, control transistors 246, 248, 250, and 252 are used to turn off the buffers and deselect their associated channels (col. 5, lines 38-47). None of the control transistors of Chang are coupled between the differential amplifiers 286-288 and the output, as claimed by Applicant.

Applicant's invention provides transistors between the differential amplifiers and the output, which advantageously provides an isolation of the base-collector capacitance of the differential amplifier transistors from the output and thus reduces the crosstalk and jitter on the output from a deselected channel. Chang's circuit isolates the deselected channels from the output line—however, in contrast, Chang does not use selection transistors between differential amplifiers and output to provide this isolation. Chang provides a whole level of buffer transistors (206-208, 210-212, etc.) between the input and the differential amplifier to provide isolation. Applicant's configuration advantageously combines, in the same transistors, selection of channels and isolation of the output from amplifier base-collector capacitance. Applicant therefore believes that claim 1 is patentable over Chang.

Claims 4-8 are dependent on claim 1 and believed patentable over Chang for at least the same reasons as claim 1, and for additional reasons. For example, claims 5, 6, and 11 recite turning off and on the selection transistors; Chang does not disclose or suggest such selection transistors between output and amplifiers, as explained above. Claim 8 recites that the first and second channels are activated and inactivated using subsets of selection transistors coupled between amplifiers and output, and which is not disclosed or suggested by Chang.

Claim 9 recites a multiplexer comprising a first channel including a first input differential amplifier coupled to a first input and a first plurality of selection transistors coupled to the first input differential amplifier, a second channel including a second input differential amplifier coupled to a second input and a second plurality of selection transistors coupled to the second input differential amplifier, and an output coupled to the first and second plurality of selection transistors. Selection inputs provided to the first and second plurality of selection transistors connects either the first channel or the second channel as active for output and the other channel as inactive. Similarly as explained above for claim 1, Chang does not disclose or suggest selection transistors which connect one channel as active and the other as inactive, and which are coupled between a differential amplifier and output, as recited in claim 9.

Claims 10-15 are dependent from claim 9, supported in Applicant's specification on page 4 and Fig. 2, and are patentable for at least the same reasons and for additional reasons. For example, claims 12-15 recite connections for the selection transistors and the output which are not disclosed or suggested by Chang.

Claims 16-20 have been added by this amendment. Claim 16 is dependent on claim 1 and claims 17-18 are patentable over Chang for at least the same reasons as claims 1 and 9, respectively. Independent claim 19 recites a method for multiplexing input signals, including providing a

differential amplifier coupled to each of a plurality of input signals, and providing a plurality of selection transistors coupled between each of the differential amplifiers and an output to isolate the collector-base capacitance of the differential amplifiers from the output. The method also includes using the selection transistors to select at least one of the input signals and differential amplifiers as active for output, and to select at least one of the input signals and differential amplifiers as inactive for output. As explained above for claim 1, Chang does not disclose or suggest providing selection transistors between differential amplifiers and the output, where the selection transistors are used to select one of the inputs and amplifiers as active for output. Claim 19 is therefore believed patentable over Chang. Claim 20 is dependent on claim 19 and is patentable over Chang for at least the same reasons as claim 19.

Applicant therefore respectfully requests that the rejection under 35 U.S.C. 102 of claims 1-15 in view of Chang be withdrawn.

The Examiner rejected claims 1-15 under 35 U.S.C. §102(b) as being anticipated by Minegishi (U.S. Patent No. 6,515,518). Applicant respectfully traverses. Minegishi discloses in Fig. 7 a circuit including differential amplifiers 1A-2A and 1B-2B, transistors 3A-6A and 3B-6B provided between the differential amplifiers and a stage of transistors 31-32, and an output 37-38 coupled to the stage 31-32. Minegishi does not disclose or suggest a multiplexer in which selection transistors are coupled between the differential pairs of transistors and the output, where a channel is selected as active or inactive by the selection transistors, as recited in Applicant's amended claim 1. In Minegishi's circuit, either channel A or channel B is made active and the other channel inactive, via selection switches 15A and 15B (col. 5, lines 26-30 and 66-67, col. 6 lines 1-5). Switches 15A and 15B are not coupled between the differential

amplifiers 1A-2A/1B-2B and the output 37-38, unlike Applicant's claim. Minegishi's other transistors, such as 3A-6A, etc., do not select the channels as active or inactive, and thus Minegishi does not disclose or suggest Applicant's invention. For example, Minegishi requires more logic levels (separate logic levels for the transistors 3-6, differential amplifiers 1-2, and the switches 15) than the invention of Applicant's claim 1. Applicant's invention advantageously combines, in the same transistors, the selection of the channels and the isolation of the base-collector amplifier capacitance from the output. Applicant therefore believes that claim 1 is patentable over Minegishi.

Claims 2-8 are dependent on claim 1 and believed patentable over Minegishi for at least the same reasons as claim 1, and for additional reasons.

Claim 9 is patentable over Minegishi for reasons similar to those explained above for claim 1. Claims 10-15 are dependent from claim 9 and are patentable for at least the same reasons and for additional reasons. For example, claims 12-15 recite connections for the selection transistors and the output which are not disclosed or suggested by Minegishi. New claims 16-18 are believed patentable for at least the same reasons as their respective parent claims. New independent claims 19-20 recites a method including providing a plurality of selection transistors coupled between each of the differential amplifiers and an output to isolate the collector-base capacitance of the differential amplifiers from the output, where the selection transistors are used to select the input signals and differential amplifiers as active/inactive for output as recited in the claim. As explained above for claim 1, Minegishi does not disclose or suggest providing selection transistors between differential amplifiers and the output, where the selection transistors are used to select one of the inputs and amplifiers as active for output. Claim 19 is therefore believed patentable over

Minegishi. Claim 20 is dependent on claim 19 and is patentable over Minegishi for at least the same reasons as claim 19.

Applicant therefore respectfully requests that the rejection of claims 1-15 in view of Minegishi be withdrawn.

The Examiner rejected claims 1-15 under 35 U.S.C. §102(b) as being anticipated by Smetana (U.S. Patent No. 6,211,721). Applicant respectfully traverses. Smetana discloses in Fig. 2 a circuit including differential pair transistors Q1-Q2, Q3-Q4, etc., coupled to cascode transistors Q49 and Q50, which are coupled to output transistors Q51 and Q52 that are coupled to the outputs Q and QN. Smetana does not disclose or suggest a multiplexer in which selection transistors are coupled between the differential pairs of transistors and the output, where a channel is selected as active or inactive by the selection transistors, as recited in Applicant's amended claim 1. In Smetana's circuit, the selection transistors are transistors Q33, Q34, ... Q48 (col. 3, lines 23-28), and these transistors are coupled between the differential amplifiers Q1-Q2 etc. and ground, not between the amplifiers and the outputs Q and QN. Smetana's other transistors, such as Q49 to Q52 and Q54-Q55, are not used for selecting which amplifier channel is active or inactive. Applicant therefore believes that claim 1 is patentable over Smetana.

Claims 2-8 are dependent on claim 1 and believed patentable over Smetana for at least the same reasons as claim 1, and for additional reasons. For example, claims 5 and 6 recite that a subset of the selection transistors between amplifiers and the output are turned off and a subset are turned on; in contrast, Smetana discloses that his transistors Q49-Q51 are not turned off based on particular channel inactive status, since these same transistors Q49-51 are connected to and used for all the channels. Claim 8 recites that the first and second channels are activated and

inactivated using subsets of the selection transistors coupled between amplifiers and output, which is similarly not disclosed or suggested by Smetana, who does not disclose such a plurality of selection transistors.

Claim 9 is patentable over Smetana for reasons similar to those explained above for claim 1. Claims 10-15 are dependent from claim 9 and are patentable for at least the same reasons and for additional reasons. For example, claims 12-15 recite connections for the selection transistors and the output which are not disclosed or suggested by Smetana. New claims 16-18 are believed patentable for at least the same reasons as their respective parent claims. New independent claims 19-20 recites a method including providing selection transistors coupled between each of the differential amplifiers and an output to isolate the collector-base capacitance of the differential amplifiers from the output, where the selection transistors are used to select the input signals and differential amplifiers as active/inactive for output as recited in the claim. As explained above for claim 1, Smetana does not disclose or suggest these features. Claim 19 is therefore believed patentable over Smetana. Claim 20 is dependent on claim 19 and is patentable over Smetana for at least the same reasons as claim 19.

Applicant therefore respectfully requests that the rejection of claims 1-15 in view of Smetana be withdrawn.

Conclusion

In view of the foregoing, Applicants submit that claims 1 and 4-20 are allowable over the cited references. Applicants respectfully request reconsideration and allowance of the claims as now presented.

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,
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Date

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